IMPERIAL COLLEGE LONDON

Design Engineering MEng EXAMINATIONS 2017

For Internal Students of the Imperial College of Science, Technology and Medicine
This paper is also taken for the relevant examination for the Associateship or Diploma

Engineering Analysis EA 1.3 - Electronics

Monday 26th June 2017   14.00 to 15.30

SOLUTIONS with comments

This paper contains NINE questions.

Attempt ALL questions.

The numbers of marks shown by each question are for your guidance only; they indicate approximately how the examiners intend to distribute the marks for this paper.

This is a CLOSED BOOK Examination.

1. Find the value of V_1 and V_2 for the circuit shown in *Figure 1*.

[10]

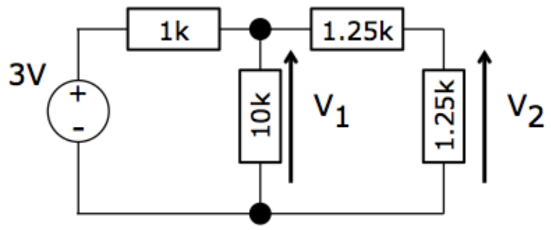
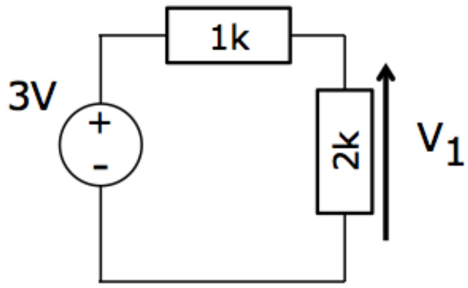


Figure 1



Solution

Find equivalent resistance of 10k // (1.25k+1.25k) = 2k:

V1 is found by considering 2k and 1k as simple voltage divider. This gives V1 = 2V.

V2 is voltage divider of V1 by two 1.25k resistor. Therefore V2 = 1V.

Comments: Most students got this question perfectly correct. A few students who did not fully understand the interaction between circuits made the same fundamental error. That is: they calculated V1 ignoring the loading effect of the two 1.25k resistors. Then use this value of V1 to calculate V2.
The class average for this question is 79%.

2. For the circuit shown in *Figure 2*, derive the equivalent resistance R_T between nodes A and B.

[10]

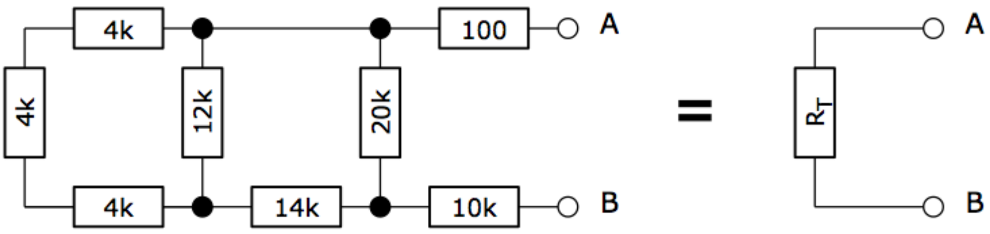
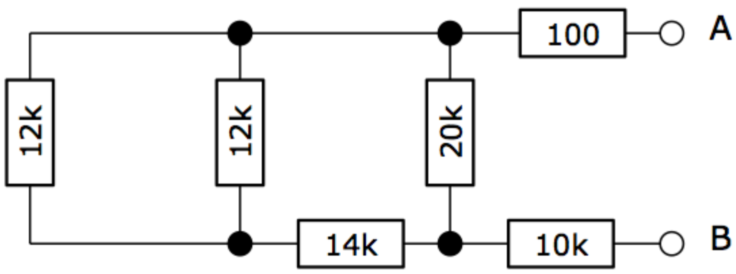


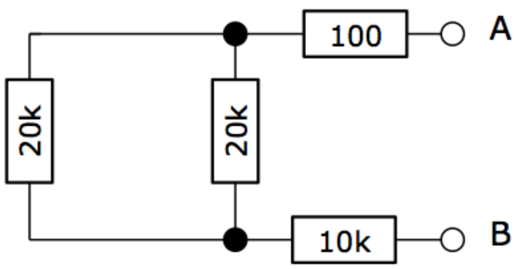
Figure 2

Solution

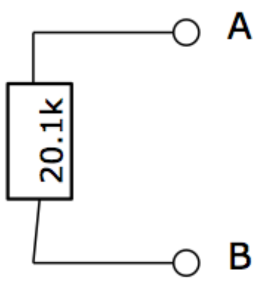
Simplify from left to right:
4k+4k+4k // 12k = 12k
This gives:



(12k // 12k) + 14k = 20k
This gives:



Finally, (20k // 20k) + 10k + 0.1k = 20.1k.



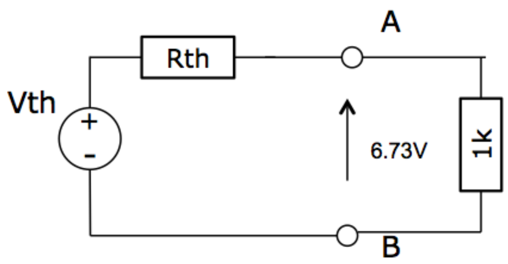
Comments: Most students got this question perfectly correct. The common mistake is to mix up series and parallel connections at later stage of the calculation.
The class average for this question is 89%.

3. An electronic circuit with two terminals A and B is known to contain a battery and a network of resistors. The voltage between A and B is measured to be 6.73V when a 1kΩ resistor is connected between the two terminals. The voltage drops to 6.17V when the resistor is reduced to 200Ω.

Derive the Thévinen equivalent circuit for the electronic circuit.

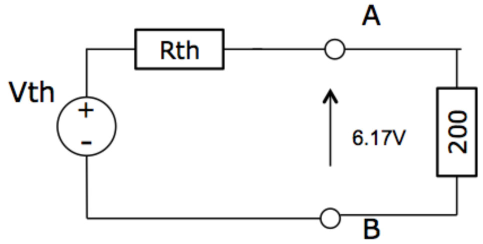
[10]

SOLUTION



This gives Eq 1:

$$6.73 = \frac{1}{1 + R_{th}} V_{th} \Rightarrow 6.73 + 6.73R_{th} = Vth$$



This gives Eq 2:

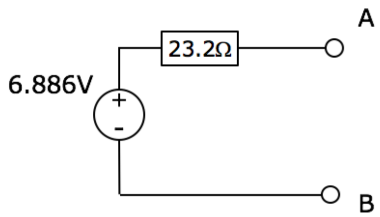
$$6.17 = \frac{0.2}{0.2 + R_{th}} V_{th} \Rightarrow 1.234 + 6.17R_{th} = 0.2\,Vth$$

$$\Rightarrow 6.17 + 30.85\,R_{th} = Vth$$

Eq 1 – Eq 2 = 0.55

$$0.56 = 24.12\,R_{th}$$

$$\Rightarrow R_{th} = 0.0232 \text{ or } 23.2\Omega.$$



Therefore Vth = 6.17 + 30.85 x 0.0232 = 6.886V.

Comment: Majority of the class could do this one. Some complicated the problem by using KCL or KVL, when a simple voltage divider equation could do perfectly.
Class average for this question is 68%.

4. The circuit shown in *Figure 4* has a 4.5V voltage source and a 20mA current source. Using the method of nodal analysis, find the value of V_X and V_Y.

[10]

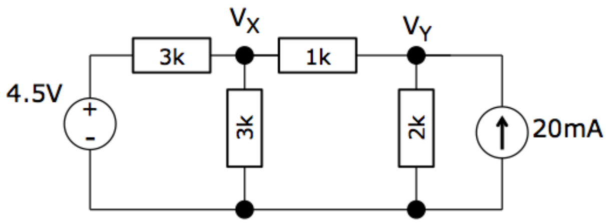


Figure 4

SOLUTION

Apply KCL at node X:

$$\frac{X-4.5}{3}+\frac{X}{3}+\frac{X-Y}{1}=0$$
$$\Rightarrow 5X-3Y=4.5$$

Apply KCL at node Y:

$$\frac{Y-X}{1}+\frac{Y}{2}-20=0$$
$$\Rightarrow -2X+3Y=40$$

Therefore, 3X = 44.5, or X = 14.83V

Y = 23.2V

Comment: Almost everyone could write down the correct simultaneous equations by applying KCL to nodes Vx and Vy. Surprisingly many could not solve simultaneous equations correctly, probably due to lack of practice. Able to write down the two simultaneous equation would attract 3 to 4 marks. The remaining marks were given depending on how much correct progress was made.

The average for this question: 82%.

5. In the circuit shown in *Figure 5*, the switch is at position 2 (i.e. opened) for a long time before moving to position 1 (i.e. closed) at time t = 0 sec.

(a) What is the capacitor voltage $v_C(t)$ at $t = 0$ sec just before the switch is closed? [2]

(b) What is the final value of v_C for $t \rightarrow \infty$? [1]

(c) What is the time constant of the function $v_C(t)$ for $t \geq 0$ sec? [3]

(d) Derive the equation for v_C as a function of time t. [4]

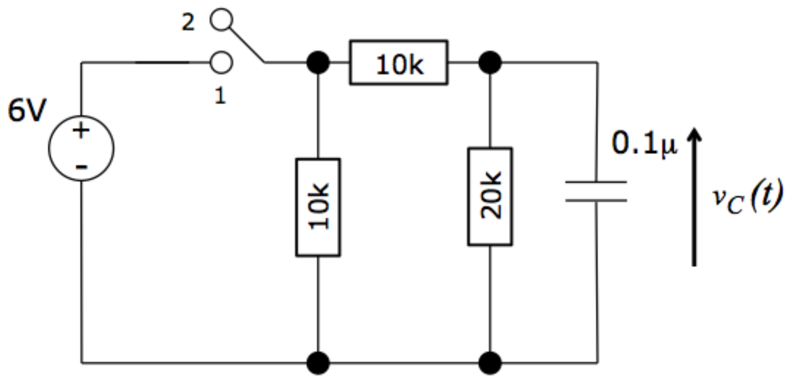


Figure 5

SOLUTION

(a) Switch in position 2 means that the circuit was NOT connected to the voltage source. $v_C(0) = 0$.

(b) When switch is closed, capacitor will charge up to value across 20k resistor as voltage divider. Therefore $v_C(\infty) = (20/(10+20)) \times 6V = 4V$.

(c) Equivalent resistance seen by capacitor when switch is closed is:

10k // 20k = 6.67k .

Therefore time constant = RC = $6.67 \times 10^{3} \times 0.1 \times 10^{-6} = 6.67 \times 10^{-4}$.

(d) $V_c(t) = 4(1 - e^{-1.5\times10^3 t})$

Comment: Most people found this question hard. Some were confused about the intial condition and got the answers to (a) and (b) mixed up. Many did not see that when switch is closed, the verticle 10k resistor is "shorted" by the 6V source and no longer play a part in the voltage or equivalent resistance calculations. Almost everyone except one person got the equivalent resistnace correctly, and therefore had the wrong time constant.
The average mark for this question is: 50%.

6. *Figure 6* shows a RLC circuit driven by a sinusoidal voltage source V_S with amplitude of 10V and a frequency of ω.

(i) Derive the complex impedance of the combined RLC circuit as a function of ω. [6]

(ii) Hence, or otherwise, derive the amplitude of the signal $V_R(t)$ across the resistor at DC and at signal frequency of 40 kHz. [8]

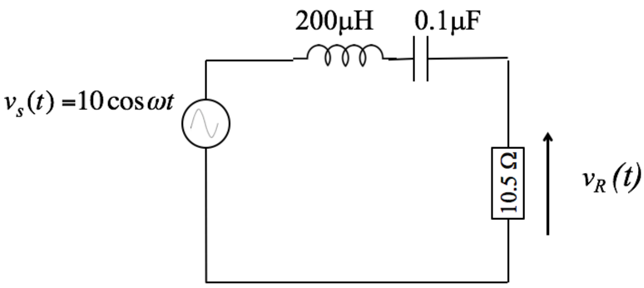


Figure 6

SOLUTION

(i) $Z = R + j\omega L + \frac{1}{j\omega C} = 10.5 + j(0.2\times 10^{-3}\omega - \frac{10^7}{\omega})$

(ii) Use voltage divider formula,

$|V_R| = 10\times\frac{10.5}{|Z|}$

at 40kHz, ω = 251327 rad/sec
Therefore
$|Z| = |10.5 + j(50.3 - 39.8)| = |10.5 + j10.5| = 14.85.$

Therefore, $|V_R| = 10\times\frac{10.5}{|Z|} = 7.07V$

Comment: Most students found this question difficult. This may be partly because of the lack of time in revision and very few opportunity to apply complex impedance in the Lab or Project. (i) should have been easy, but many spent lots of time to get to the wrong answer! (ii) is difficult. Knowing that amplitude of VR is found using the same voltage divider principle would attract 3 marks. Many student complicated the calucation using phasor, which was explicitly excluded from the course this year. Only a couple of student got the 7.07V at the end.

The class average is: 47%.

7. Given that the decimal code for the ASCII character 'A' is 65, and assuming that all numbers are represented using 8 bits, complete the missing entries that are not shaded in the following table (*Figure 7*). (No marks will be awarded for this question unless you show how the solutions are derived.)

Hexadecimal	Binary	Unsigned Decimal	ASCII
4C			
		165	

Figure 7

[10]

SOLUTION

Hexadecimal	Binary	Unsigned Decimal	ASCII
4C	**01001100**	**76**	**'L'**
A5	**10100101**	165	

Comment: This is almost a "give away" question. A few student wrote down the answer without showing any working out. They loose 5 marks because one could use a calculator to find out the answer, and that did not show understanding.

The class average is: 83%.

8. *Figure 8a* shows a two-stage amplification system that detects the presence or absence of a 20kHz ultrasonic signal through the ultrasound senor. The range of the sensor signal V_U is 20mV peak-to-peak. The required output signal V_O is 4V peak-to-peak.

   (i) Using a single supply dual operational amplifier integrated circuit with a Gain-Bandwidth Product of 800kHz, determine with justification the gain values for the two-stage of amplification.

   [5]

   (ii) *Figure 8b* shows the circuit for stage 2 of the amplification system. Assuming that the operational amplifier uses a +5V supply and is able to provide rail-to-rail output. Prove that the gain of this amplifier is given by:

   $$V_{out} = -\frac{R2}{R1}(V_{in} - 2.5) + 2.5$$

   [6]

   (iii) Hence or otherwise, design the circuit for your answer to Question 8 (i).

   [2]

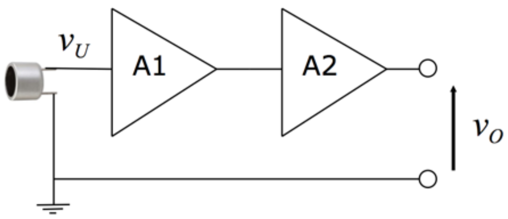


Figure 8a

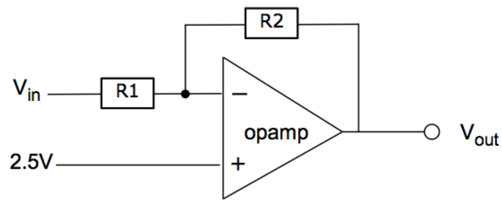


Figure 8b

SOLUTION

(i) Total gain require = 4V / 20mV = 200.

Since GBP = 800,000, the maximum gain at 20kHz would be 40.

Therefore, make A1 = 20, and A2 = 10 would work well.

(ii) The circuit works like this. Voltage at –ve input is 2.5V. Apply KCL at this node give:

$$\frac{V_{out} - 2.5}{R2} = \frac{-(V_{in} - 2.5)}{R1}$$

$$\Rightarrow V_{out} = -\frac{R2}{R1}(V_{in} - 2.5) + 2.5$$

(iii) If A2 = 10, one solution is R2 = 100k, R1 = 10k.

Comment: It is cleared that those who did Lab 3 and understood what they did also did well on this question. Most worked out that the required gain is 200 (1 mark), but many did not explain the role GBP plays – probably because did not do Lab 3! Significant number assume that the inverting amplifier gain is R2/R1 and then apply superposition. This gain a few marks, but it is NOT a proof.

The average of this question is: 54%.

9. *Figure 9* shows the relationship between the speed of a DC motor (in revolutions per minute or rpm) and the average voltage across the motor windings.

(i) Explain the advantage of controlling the speed of a DC motor with a pulse-width modulation (PWM) signal instead of a DC voltage.

[5]

(ii) A robot car uses four DC motors with a no-load speed vs drive voltage curve as shown in *Figure 9*. The wheels of the car have a diameter of 6 cm. What is the duty-cycle of the driving PWM signal if the car is to travel at a speed of 5m/sec? State any assumption used.

[8]

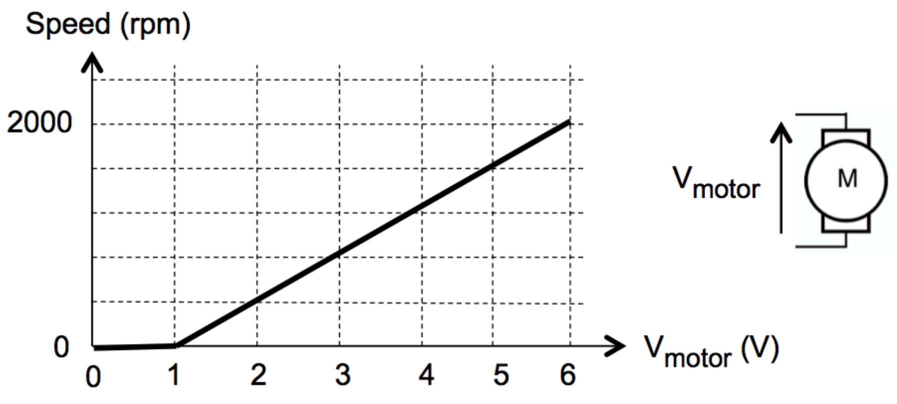


Figure 9

SOLUTION

(i) Generating a DC voltage between Vmax and 0V is generally hard to do, and may need a DAC converter. To provide enough current to drive the motor, we would need a power amplifier which is not power efficient. Using PWM requires only transistors switching between ON and OFF, and the motor "integrates" and the mean voltage on the motor is the same as duty-cycle x Vmax. This is both easy to produce and is power efficient.

(ii) 6cm wheel provides 18.85cm/rev.

Therefore 5m/sec speed requires 5/0.1885 = 26.52 rev/sec = 1591 rpm.

Therefore Vmotor = 5V x 1591/2000 + 1V = 4.98V.
Hence,
Duty cycle = 4.98/6 = 83%.

Comment: Many did not explain why PWM is advantagous. Instead only stated that you can control the average dc value, and hence the speed of the dc motor, using duty cycle. Many could not derive the solution of (ii), showing the lack of deep understanding.

The average of this question: 48%

General Comment about this paper

This turns out to be a near perfect paper. Students afterwards told me that they thought the paper was difficult bu fair. There was enough time for most students to attempt all nine questions – so I think the length and level of difficulty of the paper is about right.
The highest mark is 96% and the lowest, 34%. Furthermore, every question has someone answering perfectly and got full marks!

All these suggest that all questions are appropriate and “do-able”, and yet no one can be ignorant about this subject and got away with it by just last minute cramming. It is clear that those student who did not engage with the module generally did much worse than those who were highly engaged.

The overall average class mark is 65%. Furthermore, only 1 person failed this examination paper, but passed the module because of the Lab Oral and the Team Project marks.

